Large Current External FET Controller Type Switching Regulators

Dual-output Step-up, Negative Voltage, Step-down Switching Regulators (Controller type)

BA9743AFV, BA9744FV, BA9741F/FS

● Description

The BA9743AFV, BA9744FV, and BA9741F/FS are a 2-channel ICs, incorporating a switching regulator controller that uses a pulse width modulation. Both channels can be used for DC/DC converter operations including step up, step down, and inverting. Furthermore, since these ICs have significantly compact design, they are best suited for use as a power supply in miniature portable equipment.

● Features

1) Built-in timer-latch type short prevention circuit
2) Built-in malfunction prevention circuit during low input voltage
3) Built-in high-accuracy reference voltage output pin
   BA9743AFV 2.505V±1%
   BA9744FV 1.222V±1%
   BA9741F/FS 2.5V±4%
4) Rest period adjustable over the whole range of duty ratio
5) A wide input range provided
   BA9741F/FS/BA9743AFV VCC=3.6 to 35V
   BA9744FV VCC=2.5 to 35V

● Aplications

DC/DC converter in LCD, PC, AV, printer, DVD, projector, TV,
Fax machine, Copying machine, Measuring equipment, etc

● Product lineup

	BA9743AFV	BA9744FV	BA9741F/FS
Power supply voltage	3.6V~35V	3.6V~35V	3.6V~35V
Output pin current	100mA	30mA	100mA
Output pin voltage	Max. 35V	Max. 35V	Max. 35V
Error amplifier input voltage	0.3V~1.6V	0.3V~1.5V	0.3V~1.6V
iming capacitance	100p~15000pF	100p~15000pF	100p~15000pF
iming resistance	5.1k~50kΩ	3k~15kΩ	5.1k~50kΩ
Oscillation frequency	10k~800kHz	10k~800kHz	10k~800kHz
Operating temperature	–40°C~+85°C	–40°C~+85°C	–40°C~+85°C
Package	SSOP-B16	SSOP-B16	SOP16/SSOP-A16

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● Absolute maximum ratings

Item	Symbol	Limits				Unit
		BA9743AFV	BA9744FV	BA9741F	BA9741FS	
Power supply voltage	VCC	36	36	36		V
Power dissipation	Pd	450*3	450*3	500*1	650*2	mW
Operating temperature	Topr	–40~+85	–40~+85	–40~+85		°c
Storage temperature	Tstg	–55~+125	–55~+125	–55~+125		°c
Output pin current	Io	120*4	60*4	120*4		mA
Output pin voltage	Vo	36	36	36		V

*1 Reduce by 4.5 mW/ °C over 25°C.
(when mounted on a PCB of 50mm×50mm×1.6 mm)

*2 Reduce by 5.0 mW/ °C over 25°C.
(when mounted on a PCB of 70mm×70mm×1.6 mm)

*3 Reduce by 6.5 mW/ °C over 25°C.
(when mounted on a PCB of 70mm×70mm×1.6 mm)

*4 Should not exceed Pd- or ASO-value.

● Electrical characteristics

◎ BA9743AFV

Electrical characteristics (Unless otherwise specified, Ta=25°C and VCC=6V)

Item	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
[Reference voltage section]						
Output voltage	VREF	2.48	2.505	2.53	V	IREF=1mA
Input stability	VDLI	–	1	10	mV	VCC=3.6～35V
Load stability	VDLO	–	1	10	mV	IREF=0～5mA
[Triangular wave oscillator section]						
Oscillation frequency	FOSC	320	400	480	KHz	RRT=10kΩ, CCT=220pF
Frequency variation	FDV	–	1	–	%	VCC=3.6～35V
[Protection circuit section]						
Threshold voltage	VIT	1.48	1.64	1.80	V	
Standby voltage	VSTB	–	50	100	mV	No pull-up
Latch voltage	VLT	–	30	100	mV	No pull-up
Source current	ISCP	1.5	2.5	3.5	μA	
Comparator threshold voltage	VCT	0.95	1.05	1.15	V	5pin, 12pin
[Rest period adjustment circuit section]						
Input threshold voltage (fosc=10kHz)	VtO	1.87	1.97	2.07	V	Duty cycle = 0%
	Vt100	1.38	1.48	1.58	V	Duty cycle = 100%
ON duty cycle	DON	45	55	65	%	VREF is divided by 13kΩ and 27kΩ resistors.
Input bias current	IBDT	–	0.1	1	μA	DTC=2.0V
Latch mode source current	IDT	200	560	–	μA	DTC=0V
Latch input voltage	VDT	2.28	2.48	–	V	IDT=40μA
[Low-input-voltage malfunction prevention circuit section]						
Threshold voltage	VUT	2.23	2.53	2.83	V	
[Error amplifier section]						
Input offset voltage	VIO	–	–	6	mV	
Input offset current	IIO	–	–	30	nA	
Input bias current	IIB	–	15	100	nA	
Open loop gain	AV	70	85	–	dB	
Common-mode input voltage	VCM	0.3	–	1.6	V	VCC=3.6～35V
Common-mode rejection ratio	CMRR	60	80	–	dB	
Maximum output voltage	VOM	2.3	2.5	–	V	
Minimum output current	VOL	–	0.7	0.9	V	
Output sink current	IOI	3	20	–	mA	FB=1.25V
Output source current	IOO	45	75	–	μA	FB=1.25V
[PWM comparator section]						
Input threshold voltage (fosc=10kHz)	VtO	1.87	1.97	2.07	V	Duty cycle = 0%
	Vt100	1.38	1.48	1.58	V	Duty cycle = 100%
[Output section]						
Saturation voltage	VSAT	–	0.8	1.2	V	Io=75mA
Leak current	ILEAK	–	–	5	μA	Vo=35V
[Total device]						
Standby current	ICCS	–	1.3	1.8	mA	When output is OFF
Average current dissipation	ICCA	–	1.6	2.3	mA	RRT=10kΩ

◎ This IC is not designed to be radiation-resistant.

◎BA9744FV

Electrical characteristics (Unless otherwise specified, Ta=25°C and V_{CC}=3V)

Item	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
[Reference voltage section]						
Output voltage	V_{REF}	1.210	1.222	1.234	V	IREF=1mA
Input stability	V_{DLI}	—	3	10	mV	VCC=2.5～35V
Load stability	V_{DLO}	—	1	10	mV	IREF=0～5mA
[Triangular wave oscillator section]						
Oscillation frequency	F_{OSC}	320	400	480	KHz	RRT=5.1k,CCT=220pF
Frequency variation	F_{DV}	—	1	—	%	Vcc=2.5～35V
[Protection circuit section]						
Threshold voltage	V_{IT}	0.98	1.18	1.38	V	
Standby voltage	V_{STB}	—	50	100	mV	No pull-up
Latch voltage	V_{LT}	—	23	100	mV	No pull-up
Source current	I_{SCP}	1.0	2.0	3.0	μA	
Comparator threshold voltage	V_{CT}	0.15	0.25	0.35	V	5pin, 12pin
[Rest period adjustment circuit section]						
Input threshold voltage (fosc=10kHz)	V_{tO}	0.96	1.01	1.06	V	Duty cycle=0%
	V_{t100}	0.46	0.49	0.52	V	Duty cycle=100%
ON duty cycle	D_{ON}	45	55	65	%	
Input bias current	I_{BDT}	—	0.1	1	μA	DTC=2V
Latch mode source current	I_{DT}	390	780	—	μA	DTC=0V
Latch input voltage	V_{DT}	V_{CC}−0.5	V_{CC}−0.4	—	V	IDT=40μA
[Low-input-voltage malfunction prevention circuit section]						
Threshold voltage	V_{UT}	1.6	1.9	2.2	V	
[Error amplifier section]						
Input offset voltage	V_{IO}	—	0	6	mV	
Input offset current	I_{IO}	—	0	30	nA	
Input bias current	I_{IB}	—	15	100	nA	
Open loop gain	AV	65	85	—	dB	
Common-mode input voltage	V_{CM}	0.3	—	1.5	V	VCC=2.5～35V
Common-mode rejection ratio	CMRR	60	80	—	dB	
Maximum output voltage	V_{OM}	1.5	2.0	—	V	
Minimum output current	V_{OL}	—	0.1	0.3	V	
Output sink current	I_{OI}	1	2.1	—	mA	FB=0.75V
Output source current	I_{OO}	50	70	90	μA	FB=0.75V
[PWM comparator section]						
Input threshold voltage (fosc=10kHz)	V_{tO}	0.96	1.01	1.06	V	Duty cycle=0%
	V_{t100}	0.46	0.49	0.52	V	Duty cycle=100%
[Output section]						
Saturation voltage 1	V_{SAT}	—	0.06	0.3	V	Io=10mA
Saturation voltage 2	V_{SAT}	—	0.15	0.4	V	Io=30mA
Leak current	I_{LEAK}	—	0	5	μA	Vo=35V
[Total device]						
Standby current	I_{CCS}	—	3.6	5.0	mA	When output is OFF
Average current dissipation	I_{CCA}	—	3.9	5.6	mA	RRT=5.1kΩ

◎ This IC is not designed to be radiation-resistant.

◎BA9741F/FS

Electrical characteristics (Unless otherwise specified, Ta=25°C and V_{CC}=3V)

Item	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
[Reference voltage section]						
Output voltage	VREF	2.4	2.5	2.6	V	IREF=1mA
Input stability	VDLI	–	1	10	mV	VCC=3.6～35V
Load stability	VDLO	–	1	10	mV	IREF=0～5mA
[Triangular wave oscillator section]						
Oscillation frequency	FOSC	320	400	480	KHz	RRT=10kΩ,CCT=220pF
Frequency variation	FDV	–	1	–	%	VCC=3.6～35V
[Protection circuit section]						
Threshold voltage	VIT	1.48	1.64	1.80	V	
Standby voltage	VSTB	–	50	100	mV	No pull-up
Latch voltage	VLT	–	30	100	mV	No pull-up
Source current	ISCP	1.5	2.5	3.5	μA	
Comparator threshold voltage	VCT	0.9	1.05	1.2	V	5pin, 12pin
[Rest period adjustment circuit section]						
Input threshold voltage (fosc=10kHz)	VtO	1.79	1.97	2.15	V	Duty cycle=0%
	Vt100	1.32	1.48	1.64	V	Duty cycle=100%
ON duty cycle	DON	45	55	65	%	VREF is divided by 13kΩ and 27kΩ resistors.
Input bias current	IBDT	–	0.1	1	μA	DTC=2.0V
Latch mode source current	IDT	200	560	–	μA	DTC=0V
Latch input voltage	VDT	2.28	2.48	–	V	IDT=40μA
[Low-input-voltage malfunction prevention circuit section]						
Threshold voltage	VUT	–	2.53	–	V	
[Error amplifier section]						
Input offset voltage	VIO	–	–	6	mV	
Input offset current	IIO	–	–	30	nA	
Input bias current	IIB	–	15	100	nA	
Open loop gain	AV	70	85	–	dB	
Common-mode input voltage	VCM	0.3	–	1.6	V	VCC=3.6～35V
Common-mode rejection ratio	CMRR	60	80	–	dB	
Maximum output voltage	VOM	2.3	2.5	–	V	
Minimum output current	VOL	–	0.7	0.9	V	
Output sink current	IOI	3	20	–	mA	FB=1.25V
Output source current	IOO	45	75	–	μA	FB=1.25V
[PWM comparator section]						
Input threshold voltage (fosc=10kHz)	VtO	1.79	1.97	2.15	V	Duty cycle=0%
	Vt100	1.32	1.48	1.64	V	Duty cycle=100%
[Output section]						
Saturation voltage	VSAT	–	0.8	1.2	V	Io=75mA
Leak current	ILEAK	–	–	5	μA	Vo=35V
[Total device]						
Standby current	ICCS	–	1.3	1.8	mA	When output is OFF
Average current dissipation	ICCA	–	1.6	2.3	mA	RRT=10kΩ

◎ This IC is not designed to be radiation-resistant.

● Reference data

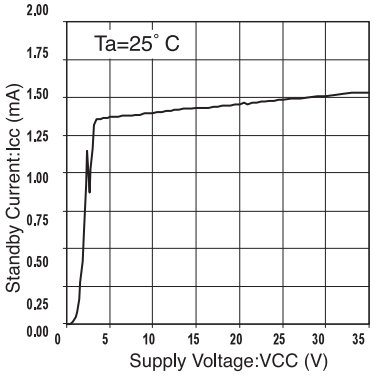


Fig. 1 Standby current vs. Power supply voltage
(BA9741F/FS/BA9743AFV)

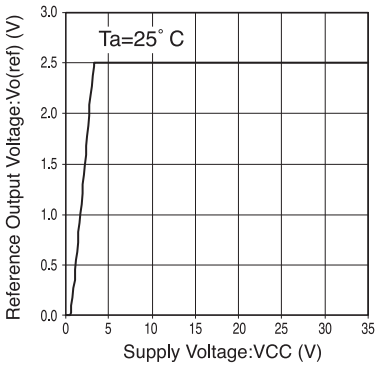


Fig. 2 Reference output voltage vs. Power supply voltage
(BA9741F/FS/BA9743AFV)

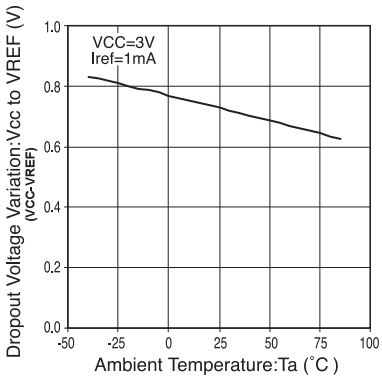


Fig. 3 Dropout voltage vs. Ambient temperature
(BA9741F/FS/BA9743AFV)

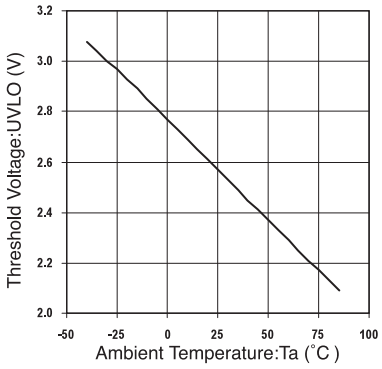


Fig. 4 UVLO operating voltage vs. Ambient temperature
(BA9741F/FS/BA9743AFV)

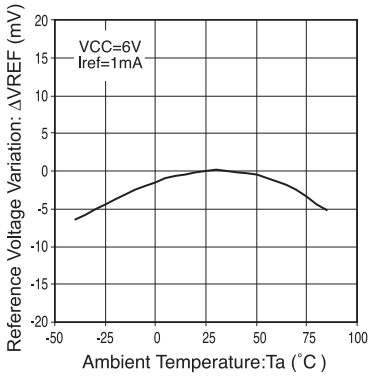


Fig. 5 Reference voltage vs. Ambient temperature
(BA9741F/FS/BA9743AFV)

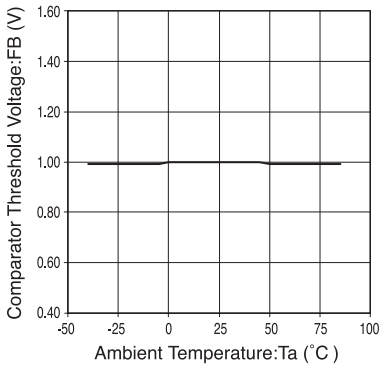


Fig. 6 Protection circuit characteristics
(BA9741F/FS/BA9743AFV)

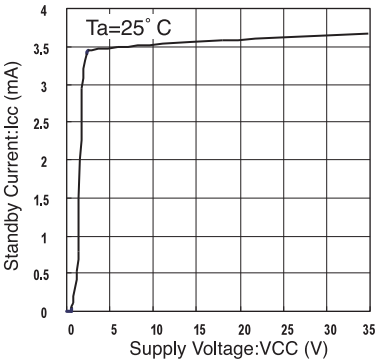


Fig. 7 Standby current vs. Power supply voltage
(BA9744FV)

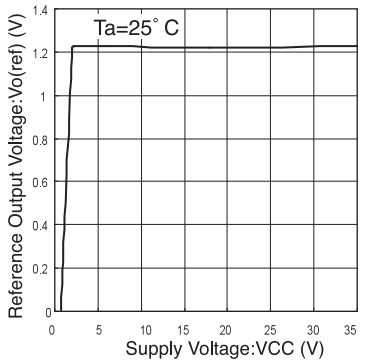


Fig. 8 Reference voltage vs. Power supply voltage
(BA9744FV)

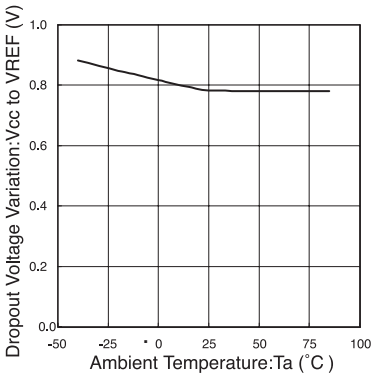


Fig. 9 Dropout voltage vs. Ambient temperature
(BA9744FV)

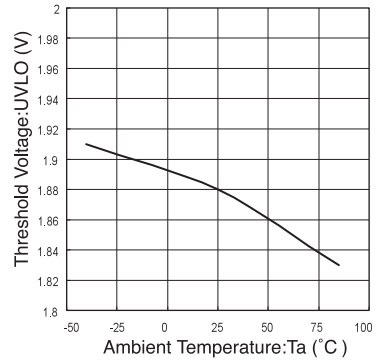


Fig. 10 UVLO operating voltage vs. Ambient temperature
(BA9744FV)

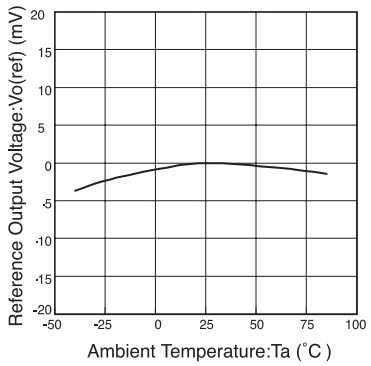


Fig. 11 Reference voltage vs. Ambient temperature
(BA9744FV)

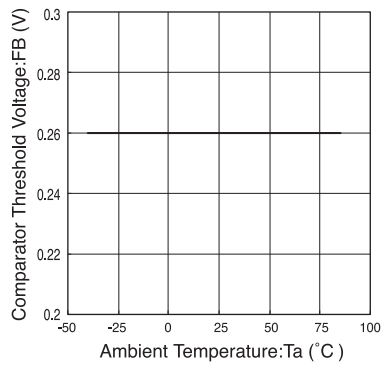


Fig. 12 Protection circuit characteristics
(BA9744FV)

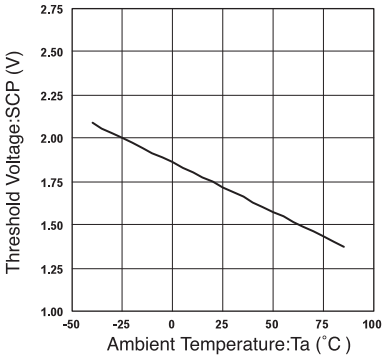


Fig. 13 Protection circuit characteristics
(BA9741F/FS/BA9743AFV)

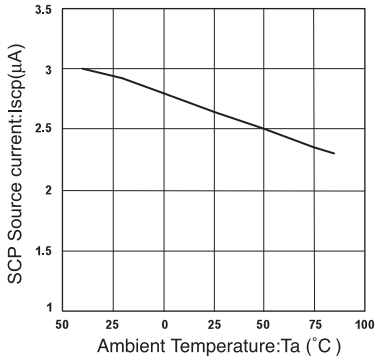


Fig. 14 Protection circuit characteristics
(BA9741F/FS/BA9743AFV)

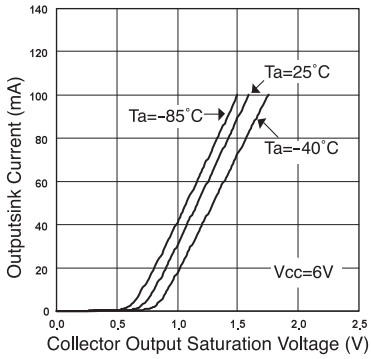


Fig. 15 Output current vs. Collector saturation voltage
(BA9741F/FS/BA9743AFV)

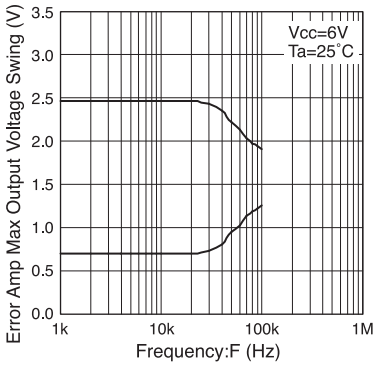


Fig. 16 Error amp. Output voltage vs. Amplitude frequency
(BA9741F/FS/BA9743AFV)

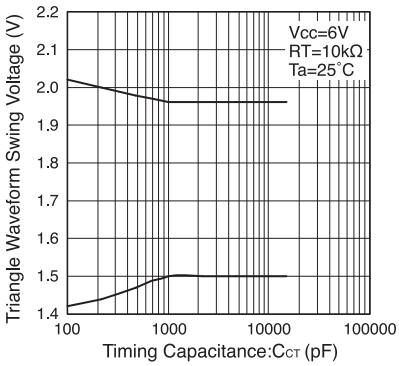


Fig. 17 Triangular wave amplitude vs. Timing capacitor
(BA9741F/FS/BA9743AFV)

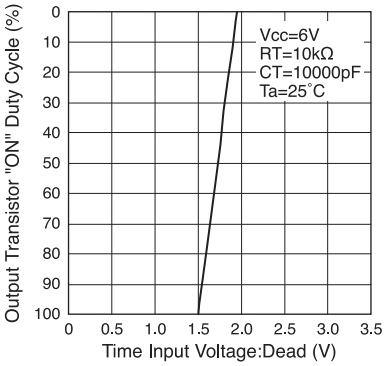


Fig. 18 Output transistor ON duty vs. Dead time voltage
(BA9741F/FS/BA9743AFV)

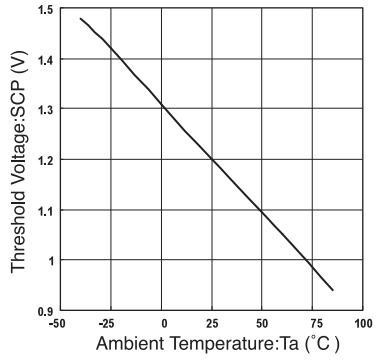


Fig. 19 Protection circuit characteristics
(BA9744FV)

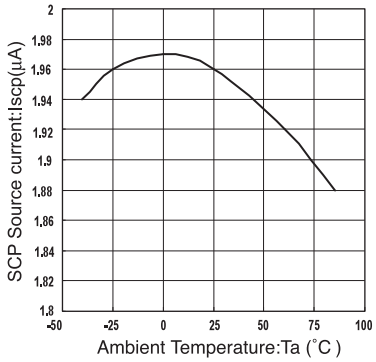


Fig. 20 Protection circuit characteristics
(BA9744FV)

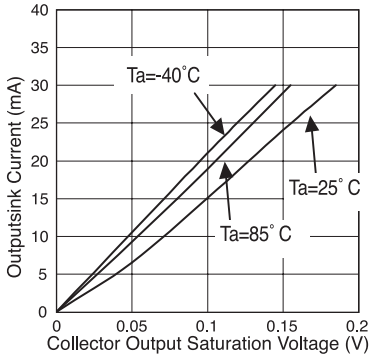


Fig. 21 Output current vs. Collector saturation voltage
(BA9744FV)

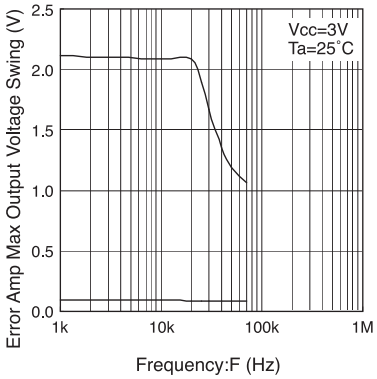


Fig. 22 Error amp. Output voltage vs. Amplitude frequency
(BA9744FV)

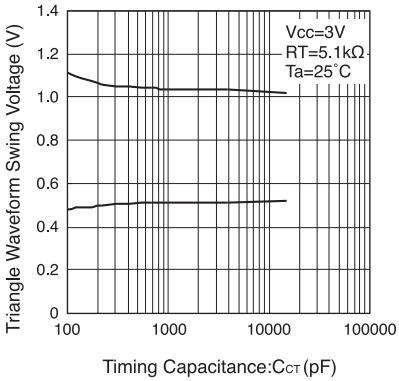


Fig. 23 Triangular wave amplitude vs. Timing capacitor
(BA9744FV)

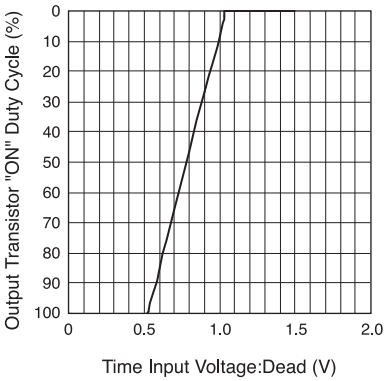


Fig. 24 Output transistor ON duty vs. Dead time voltage
(BA9744FV)

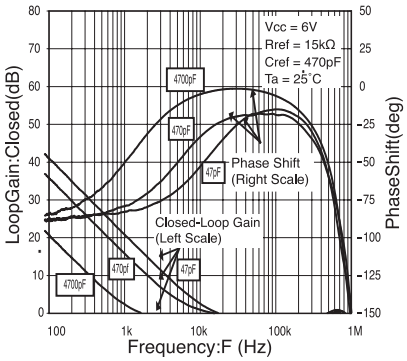


Fig. 25 Closed loop gain vs. Phase frequency (BA9741F/FS/BA9743AFV)

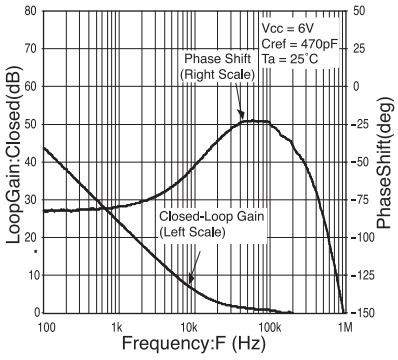


Fig. 26 Closed loop gain vs. Phase frequency (BA9741F/FS/BA9743AFV)

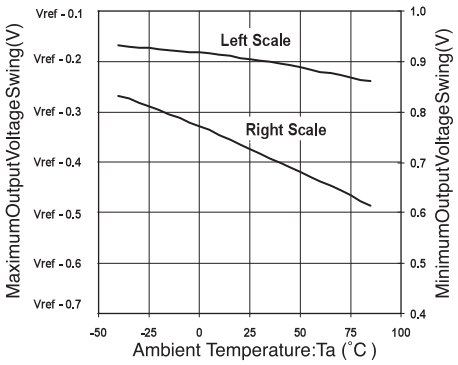


Fig. 27 Maximum output voltage amplitude vs. Ambient temperature (BA9741F/FS/BA9743AFV)

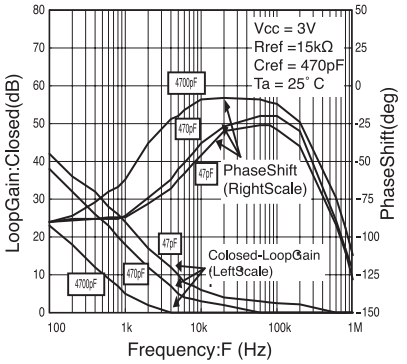


Fig. 28 Closed loop gain vs. Phase frequency (BA9744FV)

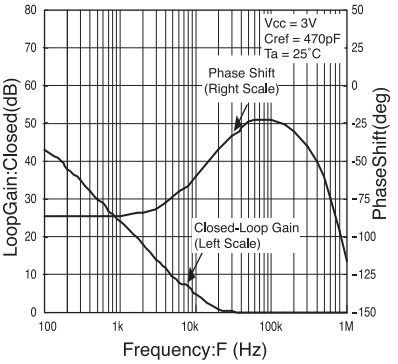


Fig. 29 Closed loop gain vs. Phase frequency (BA9744FV)

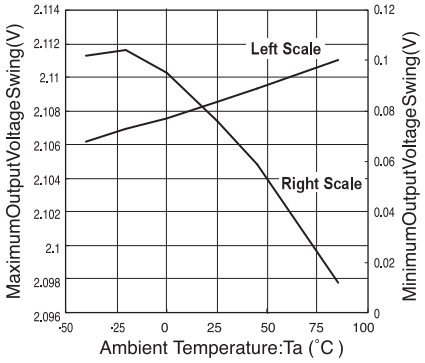


Fig. 30 Maximum output voltage amplitude vs. Ambient temperature (BA9744FV)

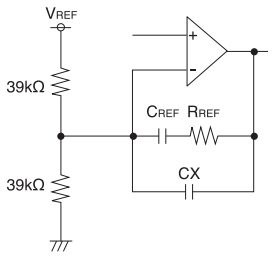


Fig.25 Test Circuit

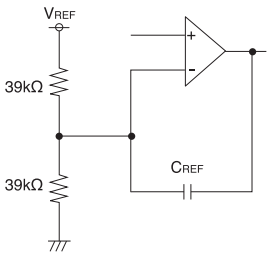


Fig.26 Test Circuit

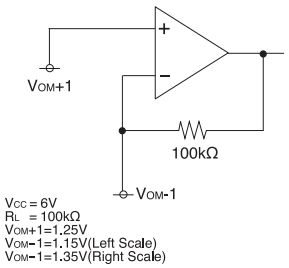


Fig.27 Test Circuit

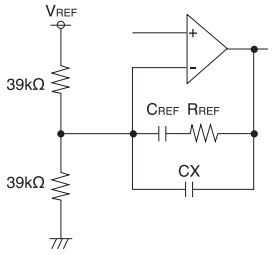


Fig.28 Test Circuit

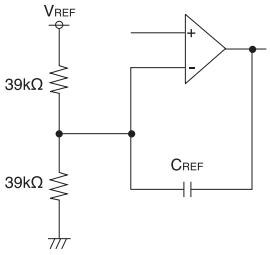


Fig.29 Test Circuit

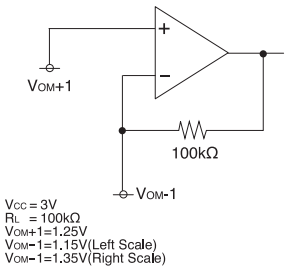


Fig.30 Test Circuit

● Block diagram/Pin assignment

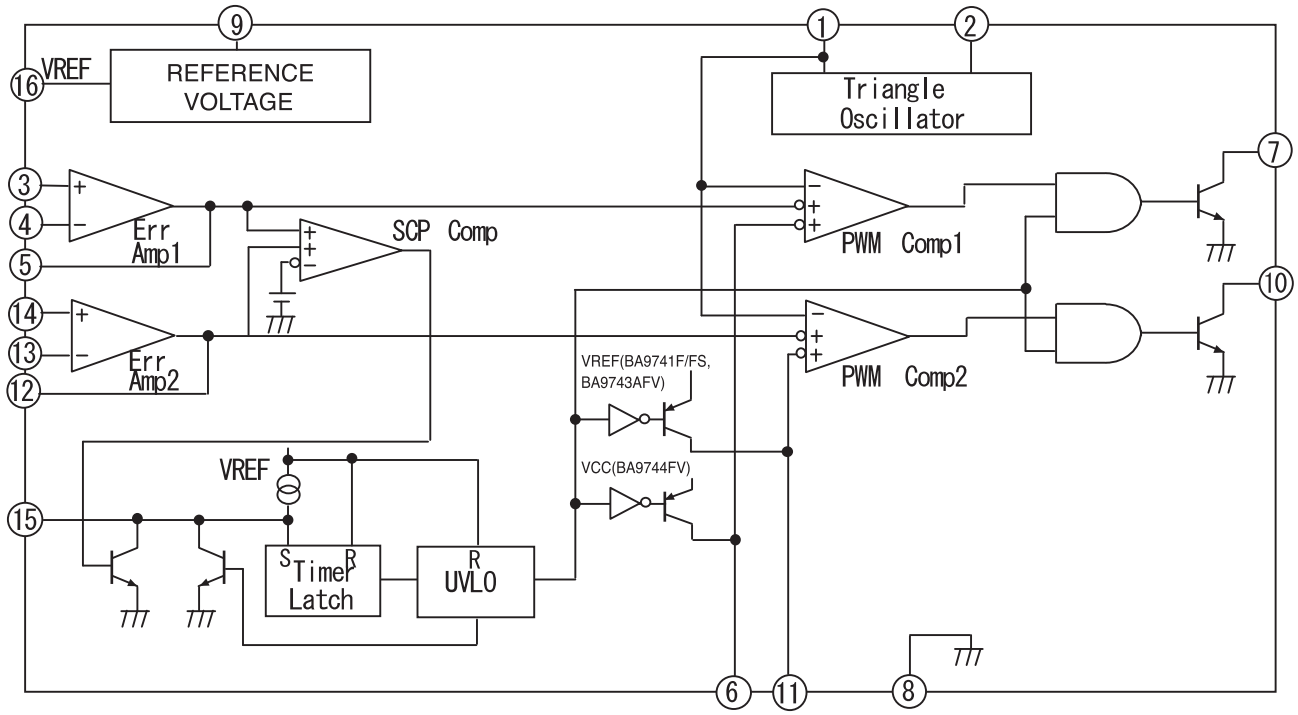
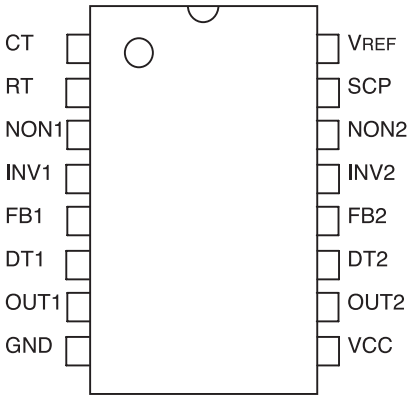


Fig.31



Pin assignment

PIN No.	Pin name	Function
1	CT	External timing capacitance
2	RT	External timing resistance
3	NON1	Positive input for error amplifier 1
4	INV1	Negative input for error amplifier 1
5	FB1	Output for error amplifier 1
6	DT1	Output 1 dead time/soft start setting
7	OUT1	Output 1
8	GND	GROUND
9	VCC	Power supply
10	OUT2	Output 2
11	DT2	Output 2 dead time / soft start setting
12	FB2	Output for error amplifier 2
13	INV2	Negative input for error amplifier 2
14	NON2	Positive input for error amplifier 2
15	SCP	Timer latch setting
16	VREF	Reference voltage output

● Description of operations

1) REFERENE VOLTAGE (Reference voltage section)

From the power supply voltage input through the VCC pin (pin 9), a reference voltage, which is stabilized at the VREF, is supplied as the operating power supply voltage for the internal circuits of the IC and, at the same time, output through the VREF pin (pin 16).

2) ErrAmp1/2 (Error amplifiers)

In the case of step up / step down application, the non-inverting input pins NON1 and NON2 are used to detect the output voltage by feeding back the voltage from the final output stage (i.e., loading side). R1 and R2, which are connected to these pins, are resistors used to control the output voltage. The voltage applied to the inverting input pins INV1 and INV2 as a reference input voltage of the error amplifiers themselves, should be the voltage obtained by dividing the reference voltage (VREF) by resistance.

$$(V_{REF}\ \frac{R4}{R3 + R4})$$

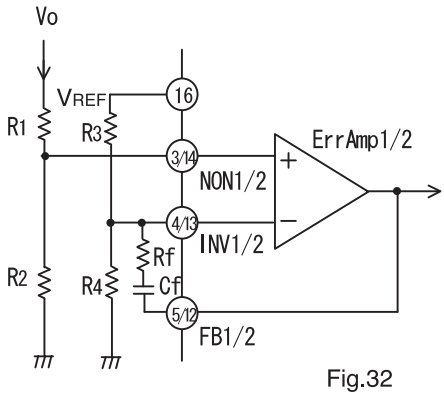


Fig.32

Furthermore, the resistor Rf and the capacitor Cf, connected between the FB1/2 (Pin 5/12) and INV1/2 (Pin 6/11), are used for feedback of the error amplifier, enabling settings of any desired level of loop gain.

It is recommended to provide AC feedback using the capacitor Cf and the resistor Rf as the feedback for the error amplifier.

The amplifier output pins FB1 and FB2 are connected to the PWM and SCP comp., and used as the non-inverting input pins.

The output voltage (Vo) setting is shown below:

$$Vo = \frac{R1 + R2}{R2} \times (V_{REF}\ \frac{R4}{R3 + R4})$$

Since the input range VOM of the NON and INV pins is 0.3V to 1.6V (for BA9741F/FS / BA9743AFV) or 0.3V to 1.5V (for BA9744FV), it is recommended to set the range to approximately VREF/2, i.e., as shown below.

$$V_{REF}\frac{R4}{R3 + R4} \fallingdotseq \begin{cases} 1.25V\ (BA9741F/FS/BA9743AFV) \\ 0.6V\ (BA9744FV) \end{cases}$$

3) Triangle Oscillator (Triangular wave oscillator section)

Used to generate a triangular waveform to be input in the PWM comp. 1/2.

The oscillator circuit charges/discharges the timing capacitor CCT that is connected between the CT pin (pin 1) and the GND at a constant current, set with resistor RRT that is connected between the RT pin (pin 2) and the GND. The triangular waveform is obtained through detecting and resetting this charged/discharged voltage.

The oscillation frequency is given through the external C_{CT} and R_{RT} pins by the formula shown below (BA9741F/FS/BA9743AFV):

(BA9741F/FS/BA9743AFV)

$fosc \fallingdotseq VRT/(2 \cdot C_{CT} \cdot R_{RT} \cdot \Delta Vosc) \fallingdotseq 1/(C_{CT} \cdot R_{RT})$

VRT: RT pin voltage 1Vtyp

ΔVosc: Triangular wave amplitude voltage=Vt0-Vt100=0.49Vtyp

(BA9744FV)

$fosc \fallingdotseq VRT/(2 \cdot C_{CT} \cdot R_{RT} \cdot \Delta Vosc) \fallingdotseq 1/(C_{CT} \cdot R_{RT})$

VRT: RT pin voltage 0.6Vtyp

ΔVosc: Triangular wave amplitude voltage=Vt0-Vt100=0.52Vtyp

However, at high frequencies, since delay in the internal circuit results in an error against the formula, set oscillation frequency according to the fosc- R_{RT} graph shown below:

Furthermore, this triangular wave can be output through the CT pin (pin 1).

Range of standard external CCT and RRT pins

R_{RT}: 5.1kΩ at minimum to 50kΩ at maximum (BA9741F/FS / BA9743AFV) or 3kΩ at minimum to 15kΩ at maximum (BA9744FV)

C_{CT}: 100pF at minimum to 15000pF at maximum

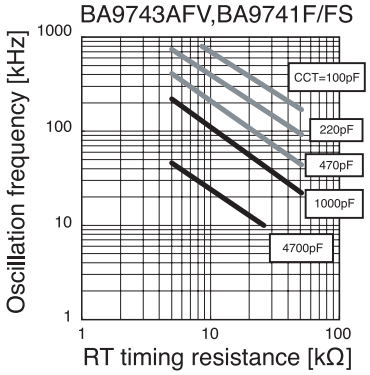


Fig.33

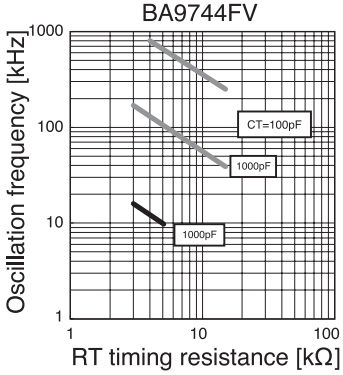


Fig.34

4) SCP Comp (Timer-latch type short-circuit prevention circuit)

When the output voltage malfunctions because of a short circuit, this function is used to turn OFF the output transistor forcedly, in order to protect the system. If the output voltage drops in realtion to the set voltage level, an error will be amplified through the Err Amp and the voltage at the FB1/FB2 pins will reach the low voltage side. If SCP Comp sets the voltage below the threshold level for either the FB1 or FB2, (i.e., 1.05Vtype for the BA9741F/FS / BA9743AFV or 0.25Vtype for the BA9744FV), the short prevention circuit will be activated to start the charging of the capacitor of SCP pin. When VIT=1.64Vtyp for the BA9741F/FS / BA9743AFV or VIT=1.18Vtyp for the BA9744FV is achieved, the output transistor will turn OFF.

The time is set by the capacitor (Cscp) connected to the SCP pin (pin 15) .
The time T_{SCP} is obtained by the formula shown below:

$$T_{SCP} = \frac{V_{IT}+V_{STB}}{I_{SCP}} \cdot Cscp$$

For example, in the case of the BA9743AFV, assuming that C_{SCP} =0.1µF, V_{IT}=1.64 V, V_{STB} =0.05V and I_{SCP} =2.5µA.

$$T_{SCP} = \frac{1.64 - 0.05}{2.5\mu} \times 0.1\mu = 63.6mS$$

In order to stop the function of the short prevention circuit, short-circuit the SCP pin to GND .

5) PWM Comp 1/2 DEAD TIME (Rest period adjustment circuit / Dead time)

This function can be set by dividing the resistance of DT1 and DT2 pins (pins 6 and 11) between V_{REF} and GND. With PWM Comp, comparing the dead time voltage input and the error voltage from the Err Amp with the triangular wave, the output drive transistors are turned ON/OFF.
When Dead time voltage>Error voltage, the output duty is determined by the dead time voltage.
The dead time voltage VDT is obtained by the expression shown below.

$$VDT = V_{REF} \cdot \frac{R2}{R1 + R2}$$

(BA9741F/FS/BA9743AFV)
When VDT=1.48Vtyp: Duty 100%
When VDT=1.97Vtyp: Duty 0%
(Provided, however, that fosc=10kHz)

(BA9744FV)
When VDT=0.49Vtyp: Duty 100%
When VDT=1.01Vtyp: Duty 0%
(Provided, however, that fosc=10kHz)

Note: If the oscillation frequency is at a high level, the upper/lower limits (Vt0/Vt100) of the triangular wave will be shifted in the direction in which the amplitude is developed.

6) PWM Comp 1/2 SS (Soft start function)

By connecting the resistors R1 and R2, and the capacitor CDT to DT pins (pins 6 and 11), as shown in figure on the right, the soft start function is enabled.

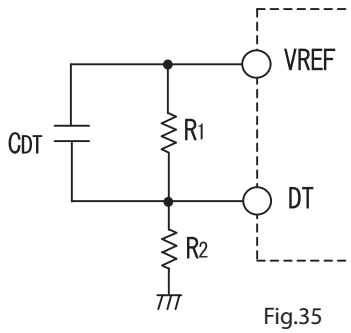
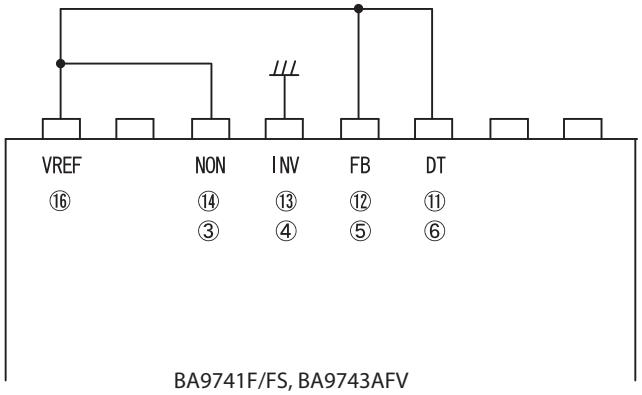
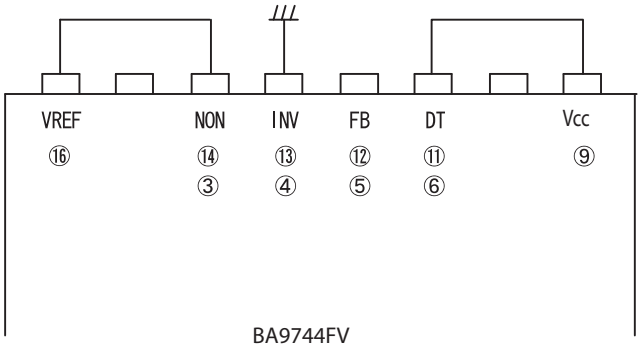


Fig.35

7) Handling of pins of unused channel



BA9741F/FS, BA9743AFV
Fig.36



BA9744FV
Fig.37

If channel 1 is only used, the unused channel should be handled as shown above.

● Typical application circuit

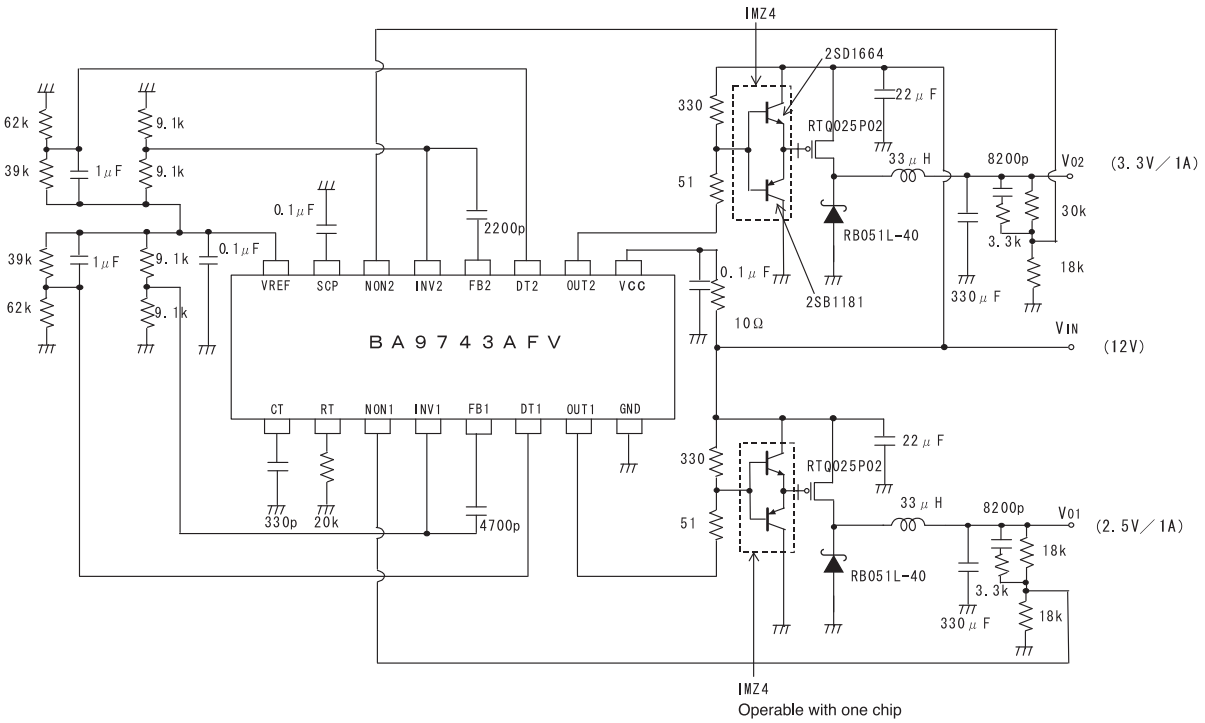


Fig. 38

1) Setting the coil (L) and capacitor (Co) of output section

The settings of the coil and capacitor with the step down application are made as shown below:.

<Setting of L value>

If the load current increases, a current will continuously flow through the coil, thus holding the relational formulas (1).

$$L = \frac{Ts}{\Delta IL} \times \frac{(VIN - Vo) \times Vo}{VIN} \quad \text{——————} \quad (1)$$

VIN : Input voltage
Ts : 1/(Oscillation frequency)
ΔIL : Ripple current of coil

ΔIL should tyically be set to 30% or less than the maximum output current (Iomax).
Increasing the L value decreases the ripple current (ΔIL). Generally, the larger the L value, the smaller the allowable current of coil. Consequently, since the ripper current exceeding the allowable current results in variations in the L value, check for the appropriate current value with the coil manufacturer.

<Setting of output capacitor Co>

The output capacitor Co should be selected according to the ESR (Electric Series Resistance) characteristics of the capacitor.
For the output ripple voltage (ΔVo), the following formula is held according to the ESR of the output capacitor:

$$\Delta Vo \fallingdotseq \Delta IL \times ESR$$

ESR: Series resistance of the output capacitor Co

A ripple component, due to the output capacitor, is significantly small in comparison to that due to the ESR.
Even though the Co value should meet the condition of $1/(3 \cdot Ts) > 1/2\pi\ (L \times Co)1/2$, it is recommended to use a capacitor with a high enough capacitance value, to meet the ESR condition.

<Switching element>

The switching element should be determined according to the peak current. The peak current Isw (peak) flowing thought the switching element is equal to that flowing through the coil, thus holding the formula shown below:

$$Isw\ (peak) = Io + \Delta IL/2$$

Select a switching element that has an allowable current that is twice (or more) as large as the peak current obtained by the formula shown above. Furthermore, with consideration given to overcurrent caused by output short-circuited, provide an application for overcurrent protection, wherever necessary.

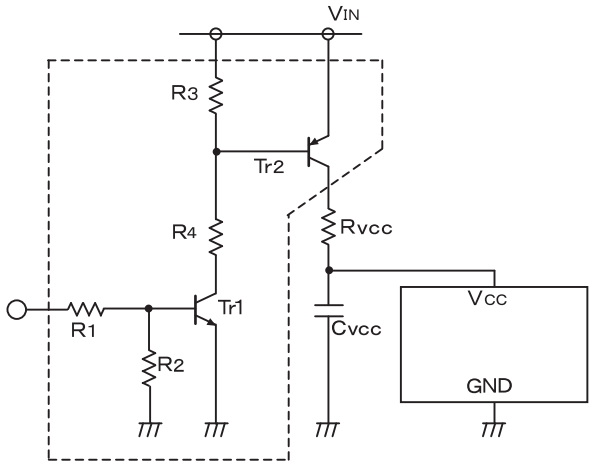
2) Typical standby circuit

The typical standby circuit is shown in the dotted frame below.

An additional switch is typically mounted between the power supply (VIN) and the IC power supply pin (VCC).

Controlling the switch so that Tr1 and Tr2 will turn OFF when the standby circuit is activated, reduces current flow in standby mode.

It is recommended to set the RVCC to 10Ω and the CVCC to 0.1μF.
Set RVCC and the CVCC within the range of 1 to 100Ω and 0.1 to 100μF.
Providing additional RVCC and CVCC helps to cut noises from the VIN line.



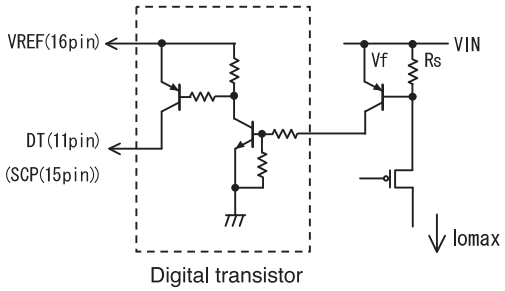
Typical standby circuit Fig.39

3) Typical overcurrent protection circuit

Insert sensing resistors between FET source and VIN of the channel P of output section, as shown in figure on the right, to detect an overcurrent.

$$Iomax = \frac{Vf}{RS}$$

If any sensing resistor detects an overcurrent, the composite digital transistor, shown in figure on the right, will turn ON to set the DT pin to “H”, thus turning OFF the output.



Typical covercurrent protection circuit Fig.40

Once the DT pin has been set to “H”, soft start (restart) mode is enabled through an external capacitor.Furthermore, if an overcurrent flows through the circuit, latching will be enabled through connecting the digital transistor PNP collector to the SCP pin (pin 15).

4) Typical application of Master/Slave operation circuit

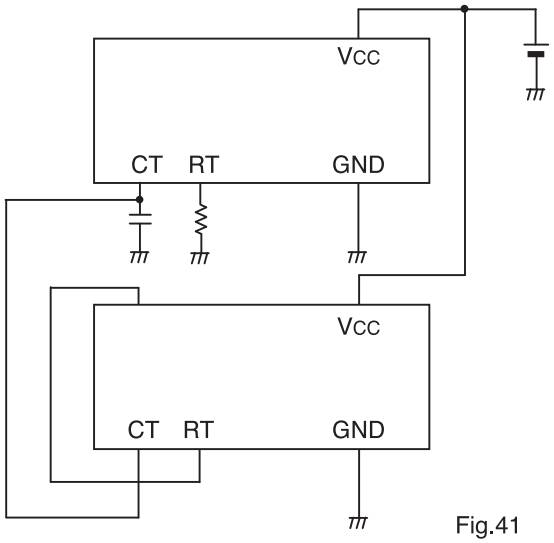


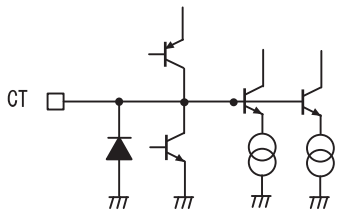
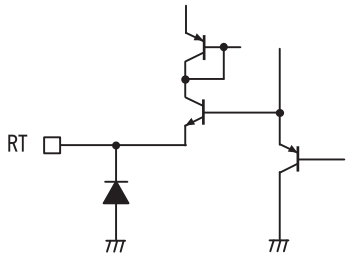
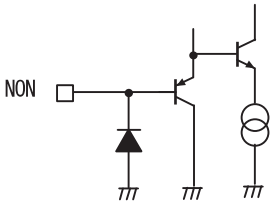
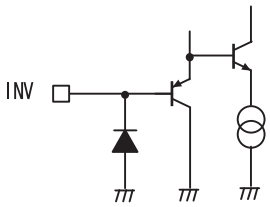
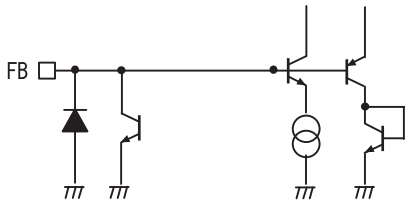
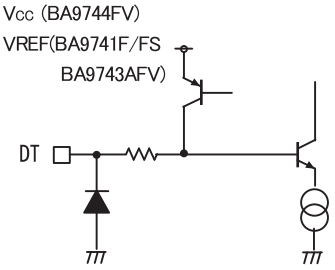
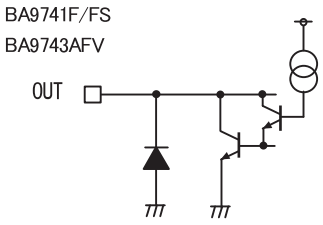
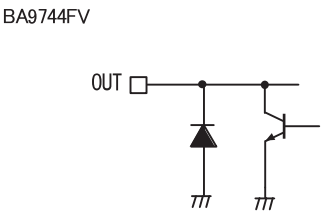
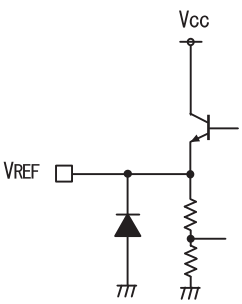
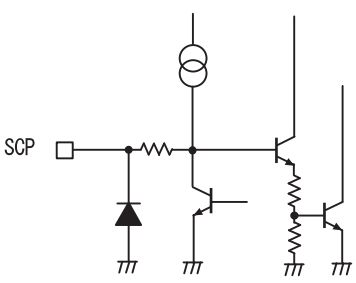
Fig.41

Caution:

The oscillation frequency should be determined according to capacitors and resistors connected to the CT pin (pin 1) and RT pin (pin 2) on the master IC.

However, increasing the number of slave ICs, increases the parasitic capacitance of these ICs in contact with the CT pin, resulting in a drift of oscillation frequency.

● Equivalent circuit

1PIN(CT)	2PIN(RT)
	
3, 14PIN(NON1, NON2)	4, 13PIN(INV1, INV2)
	
5, 12PIN(FB1, FB2)	6, 11PIN(DT1, DT2)
	
7, 10PIN(OUT1, OUT2)	7, 10PIN(OUT1, OUT2)
	
16PIN(VREF)	15PIN(SCP)
	

● Cautions on use

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) GND potential

Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including an electric transients.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Short circuit between pins and erroneous mounting

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuitís power lines.

5) Operation in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

7) Inspection with set printed circuit board

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

8) IC pin input

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements to keep them isolated. PñN junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the PñN junction operates as a parasitic diode.

When Pin B > GND > Pin A, the PñN junction operates as a parasitic transistor.

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

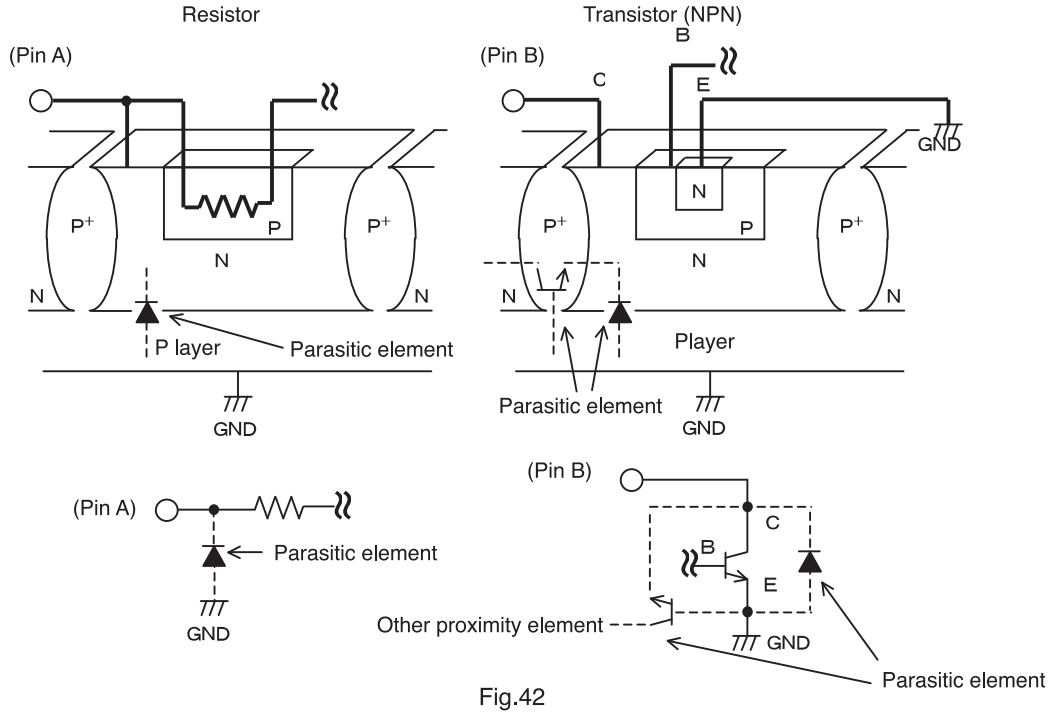
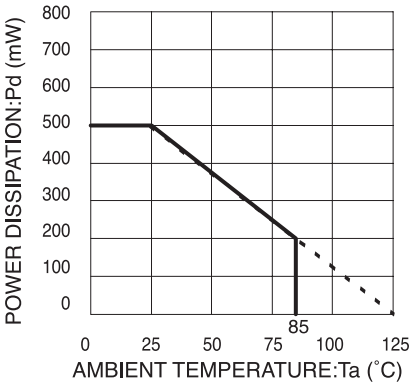


Fig.42

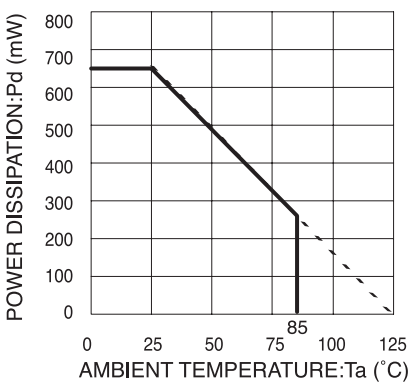
9) Common impedance

The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

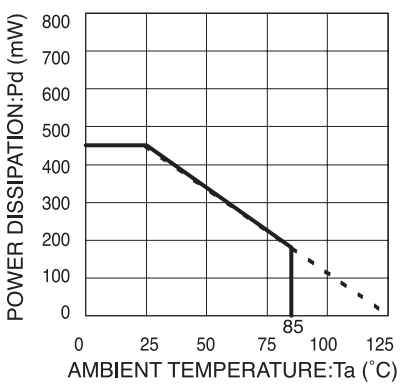
SOP16 (BA9741F)



SSOP-A16 (BA9741FS)



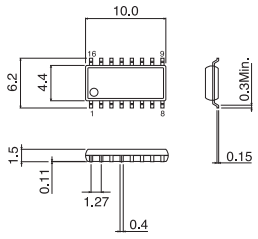
SSOP-B16 (BA9743AFV/44FV)



Note: When mounted on a printed circuit board of 70.0×70.0×1.6 mm (SOP16 and SSOP-A16)
When mounted on a printed circuit board of 50.0×50.0×1.6 mm (SSOP-B16)

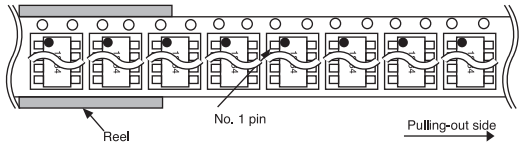
SOP16

<Outline figure>



<Package specifications>

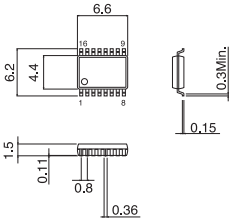
Package style	Emboss taping
Q'ty per package	2500 pieces/reel
Packaging direction	E2 (When holding a reel in left hand and pulling out the tape with right hand, No. 1 pin appears in the upper left of the reel.)



* Orders are available in complete units only.

SSOP-A16

<Outline figure>



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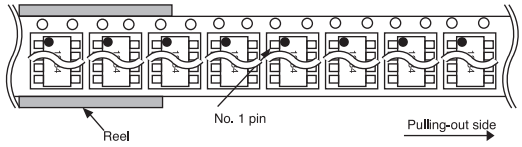

* Orders are available in complete units only.

SSOP-B16

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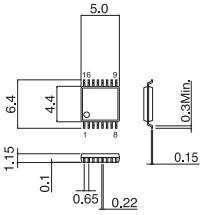

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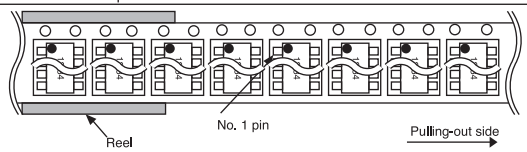

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